34B and may supply control signals to gate driver circuitry 52LB and 52RB. Gate driver circuits 52LB and 52RB may respectively handle odd and even gate lines G in lower array portion 34B.

If desired, the data lines in upper array portion 34T may be folded and the gate lines G in upper array portion 34T may be segmented into left and right halves handled by circuits 52LT and 52RT, respectively. The lower portion of display 14 may also use folded data lines and segmented gate lines if desired.

FIG. 9 is a perspective view of a portion of flexible printed circuit 56 showing how printed circuit 56 may include metal signal traces 56-1 and flexible polymer substrate 56-2. Flexible printed circuit 56 may bend about bend axis 70 during use of display 14 in device 10. Portions of flexible printed circuit 56 may, for example, extend between housing 12 and strap 16, which may allow flexible printed circuit 56 to bend as strap 16 is wrapped around the wrist of a user or it be desirable to bend flexible printed circuit 56 (by 90° or 180° or more) to accommodate mounting of flexible printed 56 within device 10 (whether or not portions of flexible printed circuit 56 extend into straps 16).

Flexible printed circuit 56 may have one or more layers of substrate material and/or encapsulant layers to help reduce stress in metal traces 56-1 (e.g., to adjust the location of the neutral stress plane for printed circuit 56 to lie within traces 56-1). Traces 56-1 may also have serpentine shapes or other shapes that help enhance trace flexibility and reduce the likelihood of cracking during bending. Traces such as traces 56-1 may have a pitch of 20-25 microns, 10-50 microns, more than 10 microns, less than 30 microns, etc. The minimum spacing between adjacent traces 56-1 may be 2-5 microns, more than 1 micron, less than 10 microns, etc. The wavelength of each trace 56-1 may be about 30-50 microns, less than 60 microns, more than 20 microns, or other suitable wavelength and each trace may have curved portions characterized by a circular radius of 5-10 microns, more than 4 microns, less than 15 microns, etc. The width of each trace 56-1 may be about 3-8 microns, more than 2 microns, less than 10 microns, etc.

FIGS. 10 and 11 show illustrative patterns that may be used for traces 56-1 on substrate 56-2. In the arrangement of FIG. 10, traces 56-1 follow sinewave-like meandering paths. In the arrangement of FIG. 11, traces 56-1 each have a series of straight segments and semicircular segments. Other layouts may be used for traces 56-1 if desired. The configurations of FIGS. 9, 10, and 11 are merely illustrative.

FIG. 12 is a circuit diagram of gate driver circuitry 52. Gate driver circuitry 52 may have the shape of a curved strip of circuitry in inactive area IA that follows the curved edge of array 34. Circuitry 52 may include shift register circuitry formed from a chain of registers such as registers 52-1. The output of each register may serve both as a gate line signal for a corresponding gate line G and as a trigger signal for a subsequent register in the chain of registers. Output drivers 52-2 (sometimes referred to as output buffers) may be used to strengthen the output of each register and to apply the strengthened version of the register output to a corresponding gate line G.

The rise and fall times of the gate line signals on gate lines G will tend to be lengthened with increasing gate line length and will tend to be decreased with increasing output driver size. Gate line loading effects (which cause rise and fall times to be extended) increase with increasing gate line length, so longer rows in array 34 that experience more loading than shorter rows will experience lengthened gate line signal rise and fall times. To compensate for the additional loading experienced when asserting gate line signals in longer rows, the strength of output drivers 52-2 can be progressively increased as a function of increasing gate line length. This type of arrangement is shown in FIG. 13.

As shown in the example of FIG. 13, gate driver circuitry 52 includes multiple gate line drivers 52-2. The strength of the driver in row R2, which has a longer gate line than row R1 is greater than the strength of the driver in row R1. Similarly, the strength of the driver in row R3, which has a gate line that is longer than the gate line in row R2 is larger than the strength of the driver in row R2. By using correspondingly larger output buffers 52-2 for longer (more heavily loaded) gate lines G, the gate line signals on all gate lines may be made to have substantially similar shapes (e.g., the rise and fall times will all be satisfactory even in displays with curved edges such as displays with circular pixel arrays 34).

The foregoing is merely illustrative and various modifications can be made by those skilled in the art without departing from the scope and spirit of the described embodiments. The foregoing embodiments may be implemented individually or in any combination.

What is claimed is:

1. A display, comprising:
display driver circuitry;
data lines coupled to the display driver circuitry;
gate lines coupled to the display driver circuitry; and
an array of pixels, wherein the pixels receive data from the display driver circuitry over the data lines and are controlled with control signals received from the display driver circuitry over the gate lines, wherein the data lines are folded data lines, wherein each folded data line has a first vertical segment that supplies data to a first column of the pixels in the array and has a second vertical segment that is coupled to the first vertical segment and that supplies data to a second column of the pixels in the array, wherein the array of pixels has left and right halves, wherein the first vertical segment in at least a given one of the folded data lines is in the left half and the second vertical segment of the given one of the folded data lines is in the right half, wherein the first vertical segment of each data line is of equal length to the second vertical segment of that data line, wherein the gate line of each row includes a left half that supplies the control signals to a left half of the pixels in that row and a right half that is electrically isolated from the left half and that supplies the control signals to a right half of the pixels in that row.

2. The display defined in claim 1 wherein the array of pixels has a curved edge.

3. The display defined in claim 2 wherein the array of pixels comprises a circular array of pixels.

4. The display defined in claim 1 wherein the display has an active area in which the array of pixels displays images and has an inactive area that does not contain any of the pixels and wherein at least some of the display driver circuitry is located in the inactive area.

5. The display defined in claim 4 wherein each data line has a coupling segment in the inactive area that couples the first vertical segment of that data line to the second vertical segment of that data line.

6. The display defined in claim 5 wherein the coupling segment of each data line is curved.

7. The display defined in claim 6 wherein the array of pixels comprises a circular array of pixels.